

ECE 545 Practice Midterm Exam Problem

Problem

Function

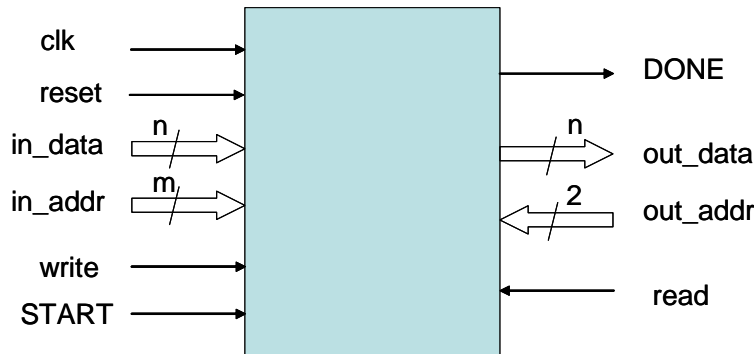
Design and describe using RTL VHDL a circuit capable of calculating the minimum, maximum, and average of k n -bit numbers, for any values of k and n which are the powers of 2, e.g. $k=8$ and $n=32$.

Optimization

Optimize your circuit for the minimum total execution time. When choosing between two circuits with the same or very similar execution time, give preference to the circuit with the smaller area.

Interface

Assume the following interface to your circuit:



Port	Width	Meaning
clk	1	System clock
reset	1	System reset – clears internal registers
in_data	n	Input data bus
in_addr	$m = \log_2 k$	Address of the internal memory where input data is stored
write	1	Synchronous write control signal
START	1	Starts the computations
DONE	1	Asserted when all results are ready
out_data	n	Output data bus used to read results
out_addr	2	01 – reading minimum 10 – reading maximum 11 – reading average 00 – high impedance at the output data bus
read	1	Synchronous read control signal

Verification

Verify your circuit using functional simulation for the case of $k=8$ and $n=32$ using a testbench capable of reading input data from a text file in the hexadecimal notation, and writing output data to a text file in the hexadecimal notation.

Suggested design steps

1. Draw a block diagram of the execution unit of your circuit
2. Draw a block diagram of a part of the control unit of your circuit
3. Describe the remaining portion of the control unit using ASM chart
4. Translate ASM chart from actions to values of specific control signals
5. Describe an interface to your circuit in VHDL
6. Translate block diagrams designed in steps 1 and 2 to VHDL
7. Translate the final ASM chart obtained in step 4 to VHDL
8. Write a testbench capable of simulating your circuit
9. Verify the operation of your circuit using functional simulation, introduce corrections in your code if necessary

Deliverables

1. All block diagrams you have developed
2. All ASM charts you have developed
3. All source codes describing your circuit
4. All testbench files, including input and corresponding output files