ECE 448: Quiz 5 Solutions

Answer given below questions:

1. Your name:

2. List four primary inputs and one primary output of the Synopsys Design Compiler:

Inputs: RTL code, standard-cell library, scripts & constraints, wireload model

Output: gate-level netlist

3. List four primary inputs and one primary output of the Synopsys Astro:

Inputs: gate-level netlist, standard-cell library, timing constraints, technology file

Output: placed & routed mask layout

4. What is a difference between an abstract view and a layout view of an ASIC library cell?

abstract view contains only information about geometrical shape and dimensions, and about location of metal pins; layout view contains additionally drawn mask layers required for fabrication.

5. What is a "zero-interconnect" timing check?

timing analysis based on the design constraints and cell delays while ignoring the RC-based interconnect delay

6. What are the two most common clock topologies aimed at reducing clock skew?

H-tree and X-tree

7. What are the three major physical quantities, obtained during timing driven placement & routing, which determine a net (interconnect) delay?

resistance of the net, capacitance of the net, and capacitance of input pins to which a given net is connected

8. What is the Design Rule Check (DRC)?

verification whether the design does not violate any fabrication rules, such as metal width, space between any two particular mask layers, etc.

9. What is the Electrical Rule Check (ERC)?

verification whether there are no any shorts or open circuits, especially involving power and/or ground, as well as transistors, resistors, capacitors with floating nodes

10. What is the name of a binary format containing the physical geometry information of the design (mask layers)?

GDS II (Graphic Design System II)