

**Practice Exam
Spring 2006
(25 points)**

**Part I (closed books, closed notes)
(30 minutes, 30 questions, 0.25 pt each, total 7.5 points)**

**Part II (open books, open notes)
(1 hr 45 minutes, 5 questions, 2x5+3x2.5 pt, 17.5 points)**

**Part I
Examples of questions**

- 1. List at least three high level languages other than C, C++, or Java that can be used to describe reconfigurable hardware:**
- 2. List at least two vendors of Reconfigurable Supercomputers:**
- 3. List at least two companies specializing in the development of commercial CAD toolsets for design of ASICs:**
- 4. Wireload model predicts of a net as a function of the net's**
- 5. Physical verification of a placed and routed ASIC includes the following three checks (give abbreviations and full names):**
- 6. A configuration file containing Process Design Rules, including the minimum metal widths and spacing is called:**
- 7. The capacities of single block RAMs used in Spartan 3 and Cyclone II families of FPGAs are equal to:

Spartan 3:
Cyclone II:**
- 8. The three memory sizes used in Stratix II FPGA devices are:**

9. List at least three functional differences between high-performance FPGA devices and low-cost FPGA devices (other than the larger size):

10. The most common DSP block built into today's FPGAs, other than a regular multiplier, is

11. The primary difference between PLA and PAL is:

12. CPLD stands for

.....
and their first vendor was

13. Frequency synthesis, i.e., the generation of clock signals with the frequency being a multiple of the original master clock frequency is done in Xilinx and Altera FPGAs using the following electronic devices:

Xilinx:

Altera:

**14. SelectMAP is a port of Xilinx FPGAs used for
and its width in bits is equal to bits**

15. Programming technology that provides the best resistance against space radiation is:

- A. SRAM**
- B. Antifuse**
- C. EEPROM**
- D. EPROM**

16. List at least three major differences between VHDL procedures and VHDL functions:

17. How to make a VHDL function global?

18. What is operator overloading?

Part II

Examples of questions

Problem 1 (5 points)

Draw a block diagram of the execution unit of the circuit capable of processing a stream of up to 2^m data bytes in search of a specific data pattern, of the size of $k=4, 8,$ or 12 bytes. The circuit should detect the pattern, and output the position of the given pattern each time it appears in the input data stream.

Port	Width	Meaning
clk	1	System clock
reset	1	System reset – clears internal registers
in_data	8	Input data stream
pattern	8	Input for the data pattern
START_pattern	1	Marks the beginning of the pattern
k=pattern_size	4	Size of the pattern
load_size	1	Load pattern size
START_data	1	Marks the beginning of the data stream
STOP_data	1	Marks the end of the data stream
last_match_pos	m	Position of the last match (0 if no previous match), counted as a position of the first byte of the matching k-byte data block
match	1	Indicates a match between a pattern and the currently processed k-byte block of the data stream
data_overflow	1	number of data bytes exceeds 2^m

Problem 2 (5 points)

Draw an ASM chart representing the operation of the control unit of the circuit from Problem 1.

Problem 3 (2.5 points)

Describe the circuit given below in VHDL using “**for generate**” statements. Label the internal signals based on your code.

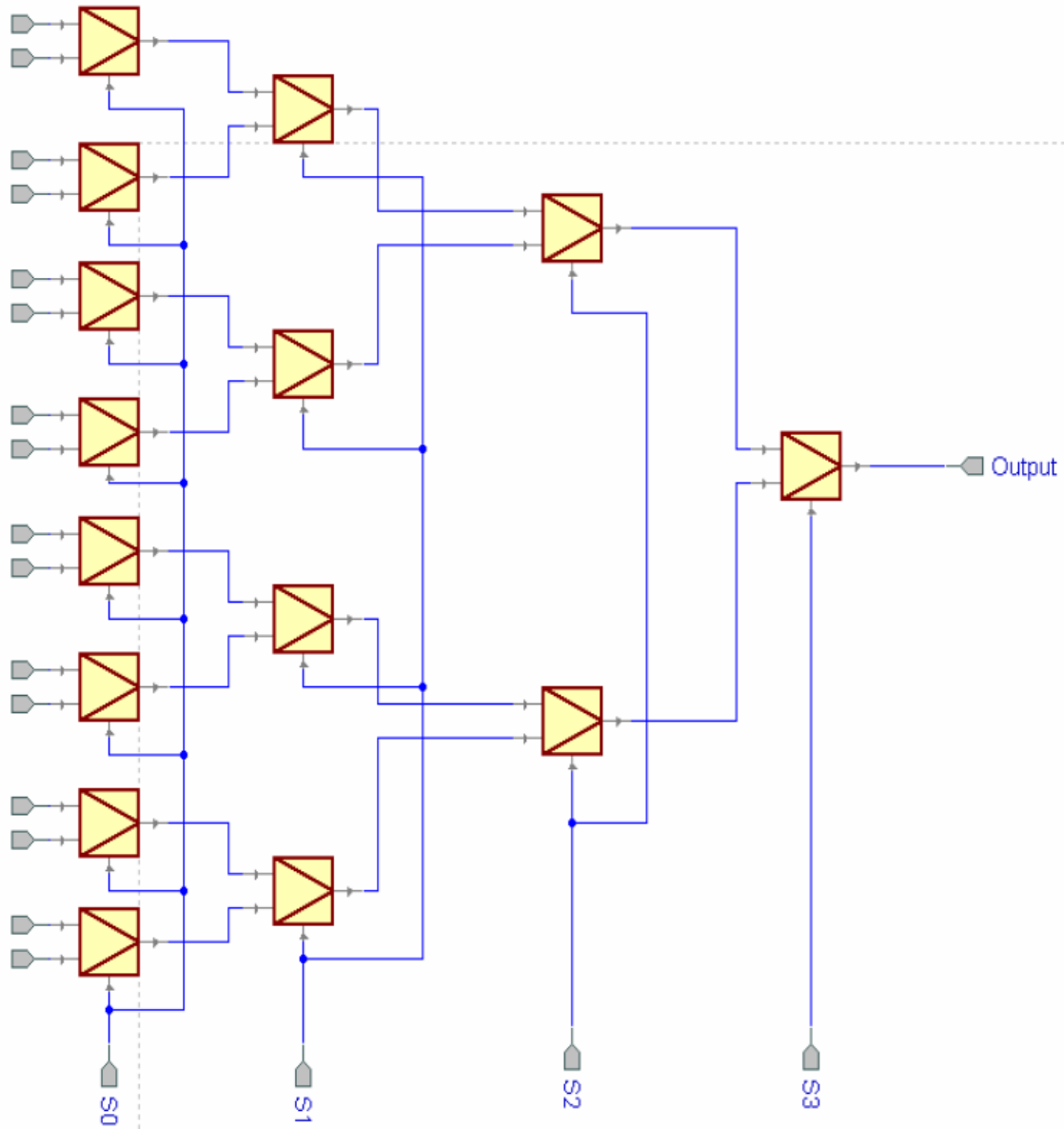
Assume that the following component is available to you:

```
entity Mux_2to1 is
    port(
        input1 : in STD_LOGIC;
        input2 : in STD_LOGIC;
        sel   : in STD_LOGIC;
        output : out STD_LOGIC
    );
end Mux_2to1;
```

architecture behavioral of Mux_2to1 is

begin

```
    output <= input1 when '0' else input2;  
end behavioral;
```



Problem 4 (2.5 points)

Modify the code of the File I/O testbench covered in Lecture 15, in such a way that it can verify the operation of a 16-bit sequential multiplier that returns results 16 clock cycles after loading operands A and B, and has the following interface.

Port	Width	Meaning
A	16	Operand A
B	16	Operand B
clk	1	Clock
reset	1	Reset
load	1	Load operands
C	32	Output $C=A*B$

Assume the following format of an input file:

load reset A B expected_C

Assume that A, B, and expected_C are provided in the hexadecimal notation.

Problem 5 (2.5 points)

Translate the following block diagram to VHDL, assuming that a generic memory and a generic register have been already defined for you in separate files.

