

**Final Exam  
Spring 2006  
May 11, 2006  
(25 points)**

**Part II (open books, open notes)  
(1 hr 45 minutes, 5 questions, 2x5+3x2.5 pt, 17.5 points)**

**Problem 1 (5 points)**

Draw a block diagram of the execution unit of a circuit capable of storing 17 8-bit values in an internal memory, and then computing in parallel:

- a. the position of a largest number in the set
- b. the second largest number in the set
- c. an average of all numbers except the largest number in the set.

Assume the following interface to your circuit:

Port	Width	Meaning
clk	1	System clock
reset	1	System reset – clears internal registers
Rdata	8	Data input
Raddr	5	Address to which input data is loaded during initialization
RWrite	1	External write
START	1	Start of computations
DONE	1	Completion of computations
Pos_max_avr	2	Choice between reading the position of the largest, value of second largest, and an average of numbers from the set
Rout	8	Result of computations

**Problem 2 (5 points)**

Draw an ASM chart corresponding to the following pseudocode:

```
for (i=0; i<32; i++)
  Memory(i) = Data
for (i=0; i<16; i++)
{
  Tmp1 = Memory(i)
  Tmp2 = Memory(32-i)
  Memory(i) = Tmp2
  Memory(32-i) = Tmp1
}
```

Express all operations in terms of active values of control signals of components involved in these operations.

**Problem 3 (2.5 point)**

The following simple processor takes up to three clock cycles to execute a single instruction.

Determine the number of clock cycles necessary to perform each of the following operations:

Operation 1:  $R1 \leftarrow \text{Data}$

Operation 2:  $R2 \leftarrow \text{Data}$

Operation 2:  $R3 \leftarrow R1 - R2$

Operation 3:  $\text{Bus} \leftarrow R3$

For each clock cycle within each operation list names of all control signals that should be active during the execution of this instruction (assume that all enable signals are active with 1, and  $\text{AddSub} = 0$  means addition,  $\text{AddSub} = 1$  means subtraction).



