

Introduction to Xilinx Virtex FPGA devices



Outline

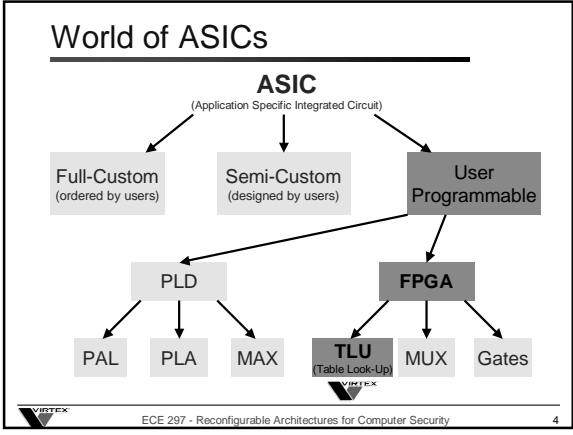
- Introduction
- Features of Xilinx Virtex FPGAs
- Architecture overview
- CLB
- Routing
- IOB
- Block SelectRAM
- Additional components

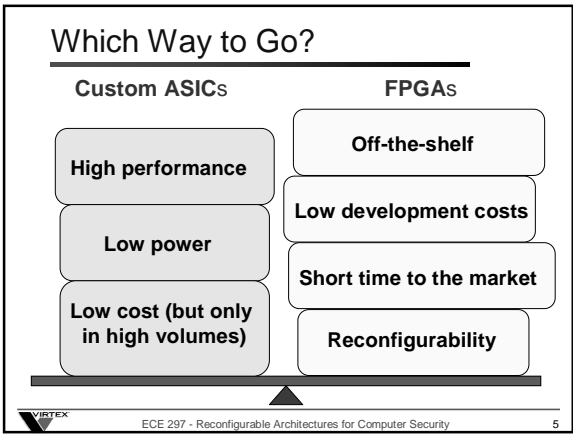


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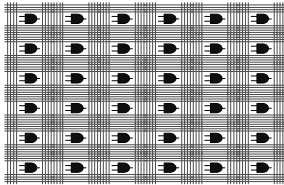




- ### Other FPGA Advantages
- Manufacturing cycle for ASIC is very costly, lengthy and engages lots of manpower
 - Mistakes not detected at design time have large impact on development time and cost
 - FPGAs are perfect for rapid prototyping of digital circuits
 - Easy upgrades like in case of software
 - Unique applications
 - reconfigurable computing
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What is FPGA?

- FPGA – Field Programmable Gate Array
 - Originally a large array of gates with programmable interconnections



- Now much more complex arrays of various components



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Xilinx Virtex 2.5V (1)

- Densities from 50k to 1M gates
- System performance up to 200MHz including I/O
- 66MHz PCI compliant
- Support 16 high-performance interface standards
- Built-in clock management circuitry
- Hierarchical memory system
- Flexible architecture
 - fast carry chain
 - multiplier support
 - cascade chain for wide-input functions
 - abundant registers/latches
 - internal 3-state bussing
 - IEEE 1149.1 boundary-scan
- SRAM-based in-system configuration
- 0.22 μ m 5-layer metal process



Virtex 2.5V Architecture (2)

- CLBs provide the functional elements for constructing logic
- IOBs provide interface between the package pins and the CLBs
- Block RAMs – dedicated dual-port memories of 4096 bits
- DLLs for clock-distribution delay compensation

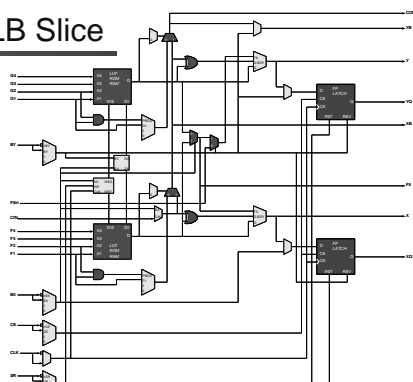


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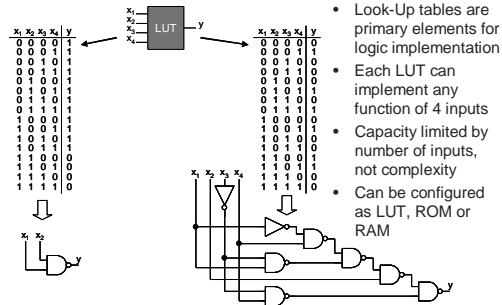
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CLB Slice



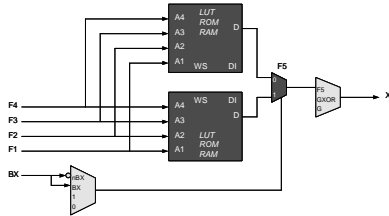
LUT Functionality



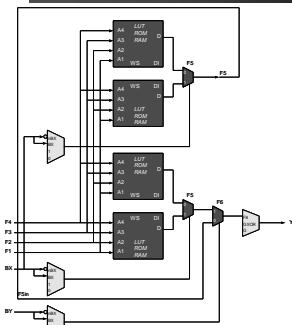
- Look-Up tables are primary elements for logic implementation
- Each LUT can implement any function of 4 inputs
- Capacity limited by number of inputs, not complexity
- Can be configured as LUT, ROM or RAM

5-Input Functions on LUTs

- One CLB Slice can implement any function of 5 inputs
- Logic function is partitioned between two LUTs
- F5 multiplexer selects LUT



6-Input Functions on LUTs



- One CLB (two adjacent Slices) can implement any 6-input function
- Logic function is partitioned among four LUTs
- Dedicated multiplexers F5 and F6 select LUT

RAM 16x2 on LUT

- Each LUT can implement a 16x1 RAM
- Inputs to RAMs are through *BY* and *BX*
- Both RAMs share CLK and WE

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RAM 32x1 on LUTs

- Both LUTs share inputs
- Input *BX* acts as *A5*
- Input *BY* is an input to the RAM

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RAMD 16x1 (Dual-Port)

- One port used for writing and reading, other only for reading
- Writing to both memories simultaneously

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Carry Chain

- Carry chain connects CLB Slices in the same column
- Chain is unidirectional
- Can connect only as many CLB Slices as there are rows in the device (64 in XCV1000)
- Very useful for implementing arithmetic logic

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Ripple-Carry Adder

- Full adder implemented using *propagate/generate* idea
- Carry is propagated from the previous stage to the next stage only when it is necessary i.e. *A* and *B* have different values. Function *p* decides if carry needs to be propagated
- Function *g* generates carry when carry does not get propagated.

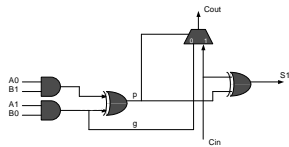
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Ripple-Carry Adder on CLB Slice

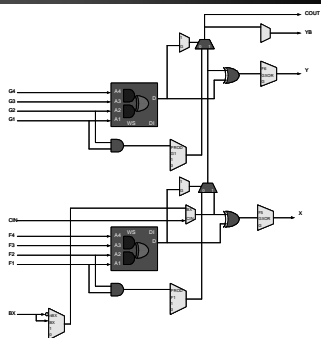
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Array Multiplier

- Implementation of array multiplier requires addition of multiple products
- Can be implemented on full adders with inputs from AND gates computing products



Array Multiplier on CLB Slice

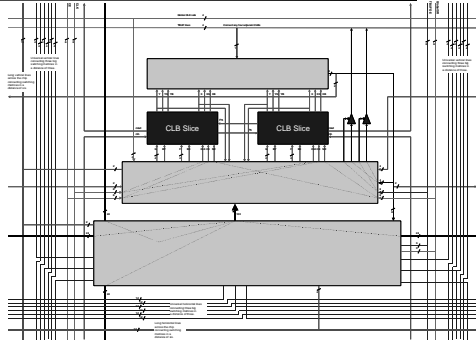


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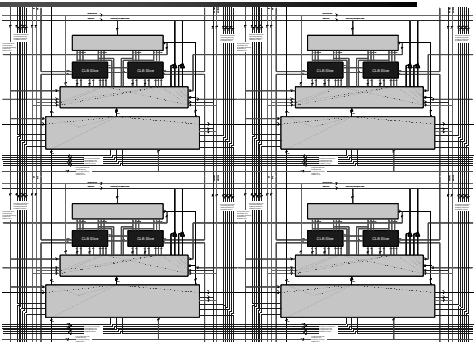
Routing Between CLBs (1)



Routing Between CLBs (2)

- Routing resources organized into a hierarchy of nets
 - carry chain directly connects adjacent CLB Slices in the same column
 - 2 dedicated nets connect adjacent CLB Slices in the same row
 - 24 nets in each direction connect adjacent routing matrices
 - 48 vertical nets and 72 horizontal nets connect every 3rd routing matrix
 - 12 vertical and 12 horizontal lines connect every 6th routing matrix across the entire chip
- Dedicated CLK, RST, CE and 3-state nets

Routing Between CLBs (3)

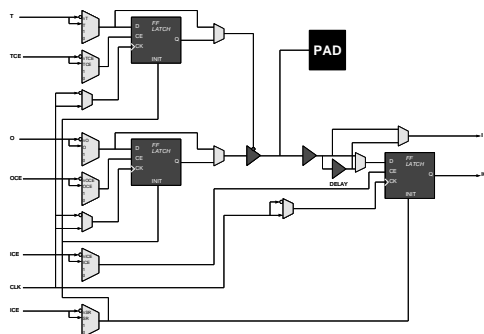


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IOB Details



IOB Functionality

- IOB provides interface between the package pins and CLBs
- Each IOB can work as uni- or bi-directional I/O
- Outputs can be forced into High Impedance
- Inputs and outputs can be registered
 - advised for high-performance I/O
- Inputs can be delayed to achieve 0 ns hold time



Supported I/O Standards

Vcco	Compatible Standards
3.3V	PCI, LVTTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+, LVPECL
2.5V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+, BLVDS, LVDS
1.8V	LVCNOS18, GTL, GTL+
1.5V	HSTL I, HSTL III, HSTL IV, GTL, GTL+



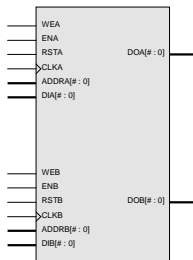
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Block SelectRAM

- Dedicated 4kb dual-port RAM memory with variable input/output widths
- Both ports completely independent
- Writing and reading allowed on both ports
 - writing from both ports to the same location results in ambiguity



Port Configurations

- Each port can be configured independently
 - perfect for bus-width conversion and clock domain change

Width	Depth	ADDR Bus	Data BUS
1	4096	[11 : 0]	[0]
2	2048	[10 : 0]	[1 : 0]
4	1024	[9 : 0]	[3 : 0]
8	512	[8 : 0]	[7 : 0]
16	256	[7 : 0]	[15 : 0]



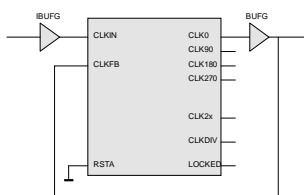
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Delay Locked Loop

- Four fully digital DLLs provide
 - compensate clock routing delays
 - low clock skew
 - advanced clock domain control



Features of DLL

- Can shift phase of the input clock by 0, 90, 180 or 270 degrees
- Can multiply input clock by 2
- Can divide input clock by 1.5, 2, 2.5, 3, 4, 5, 8 or 16
- Can correct duty cycle of the input clock



Startup Virtex

- Startup Virtex is used for Global Set/Reset and Global 3-state control
- When GSR is High all flip-flops, latches and Block SelectRAMs within device get set/reset to initial state
- When GTS is High all IOB outputs are forced into High Impedance

