

Introduction to FPGA Tools



Complete FPGA Implementation Environment











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FPGA Design Process(1)

Functional simulation is a logic-level simulation that is used to verify the logic functionality of the design before synthesis. It is the only simulation that can be used to verify the logic functionality of the design before synthesis.

Specification

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VHDL description

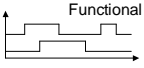
```

entity AND2 is
    port (
        A : in std_logic;
        B : in std_logic;
    );
    Y : out std_logic;
end entity AND2;

architecture AND2_ARCH of AND2 is
    Y <= A and B;
end architecture AND2_ARCH;
                    
```

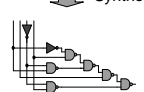
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Functional simulation



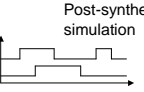
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Synthesis



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Post-synthesis simulation




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FPGA Design Process(2)

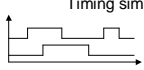
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Placement & Routing




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Timing simulation




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Bitstream Generation

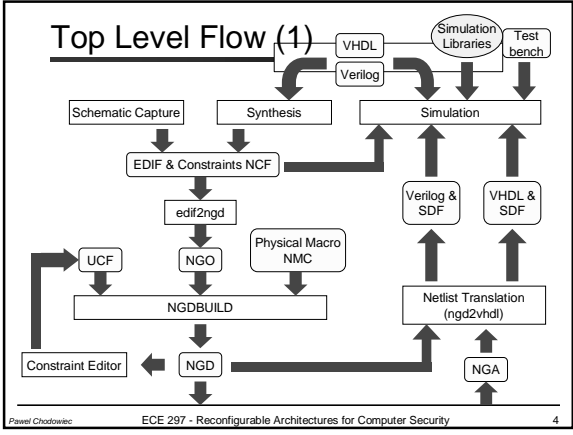


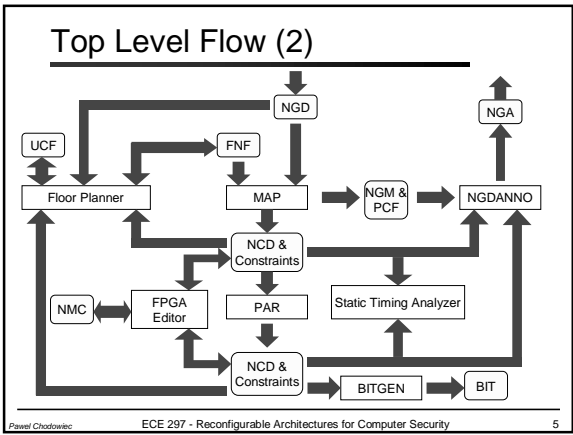
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On chip testing



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Simulation Tools

Active-HDL™
Complete FPGA Verification Environment

ModelSim®

Mentor Graphics

Many others...

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Features of Simulation Tools (1)

- Can perform simulation on different stages of design
 - Functional simulation
 - Post-synthesis simulation
 - Post-mapping simulation with preliminary timing information
 - Post-PAR simulation with detailed timing information
- Simulate VHDL, Verilog or EDIF

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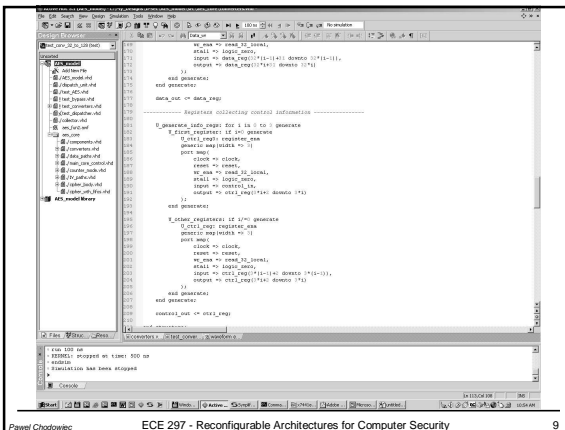
Features of Simulation Tools (2)

- Timing simulations require SDF files (Standard Delay File)
- Excellent design entry tools
 - Greatly support RTL code development and verification
- DO NOT perform any synthesis nor compilation

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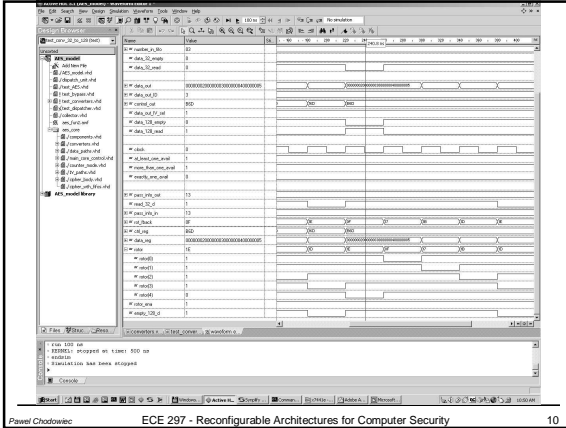
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Synthesis Tools

... and others

Features of synthesis tools

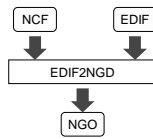
- Interpret RTL code
- Produce synthesized circuit in standard EDIF format
 - EDIF contains low level circuit description in terms of primitive objects native to particular FPGA
- Some can give preliminary performance estimates
- Some can show circuit schematics in RTL and optimized levels

edif2ngd



- Command line tool
- Translates EDIF and NCF files to NGO file

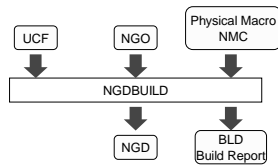
- Think of NGO file as of an object file



ngdbuild



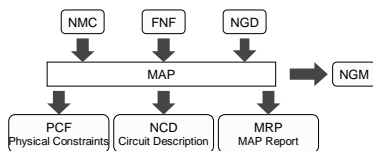
- Command line tool
- Build the entire design from many pieces
- Collects information from all NGO, NMC and UCF files and puts it in NGD (Native Generic Database) file




map

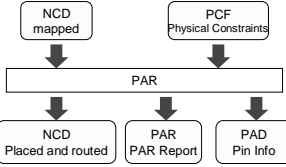


- Command line tool
- Maps a logical design to a Xilinx FPGA



par 


- Command line tool
- Places and Routes the design
 - All FPGA components get assigned to particular locations and all nets get routed



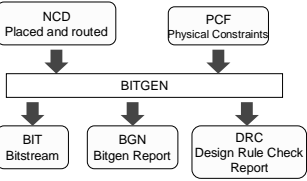
```

graph TD
    A[NCD mapped] --> B[PAR]
    C[PCF Physical Constraints] --> B
    B --> D[NCD Placed and routed]
    B --> E[PAR PAR Report]
    B --> F[PAD Pin Info]
  
```

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bitgen 


- Command line tool
- Produces configuration bitstream



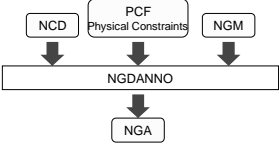
```

graph TD
    A[NCD Placed and routed] --> B[BITGEN]
    C[PCF Physical Constraints] --> B
    B --> D[BIT Bitstream]
    B --> E[BGN Bitgen Report]
    B --> F[DRC Design Rule Check Report]
  
```

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ngdanno 

- Command line tool
- Generates a generic timing simulation model



```

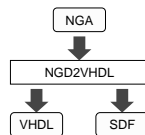
graph TD
    A[NCD] --> B[NGDANNO]
    C[PCF Physical Constraints] --> B
    D[NGM] --> B
    B --> E[NGA]
  
```

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ngd2vhdl



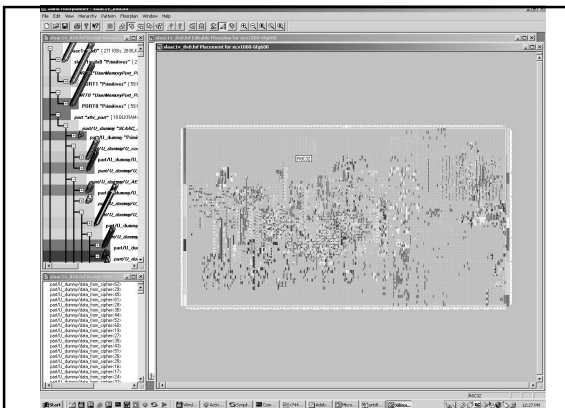
- Command line tool
- Translates back-annotated simulation model to VHDL

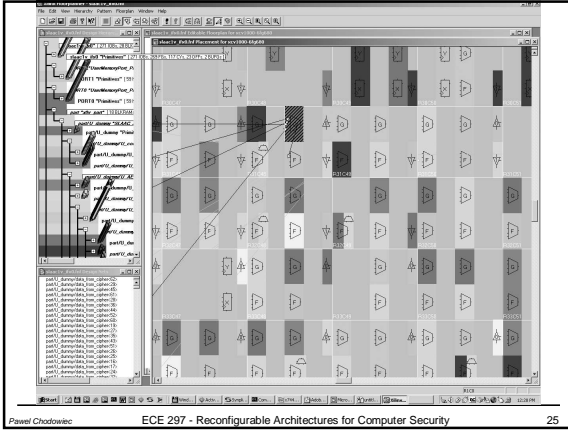


Floorplanner



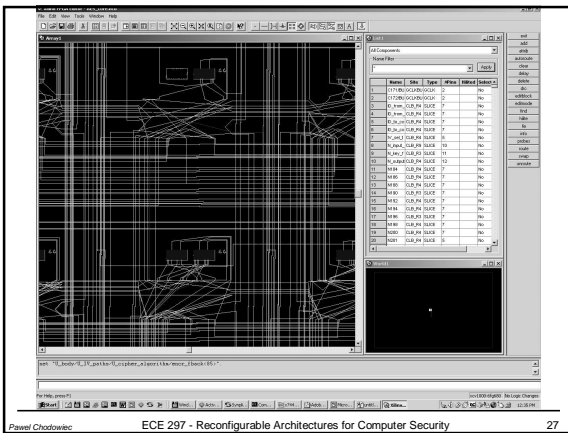
- Supports hand-placement of FPGA components
- Creates FNF or UCF file
- Some components like DLLs need to be placed manually

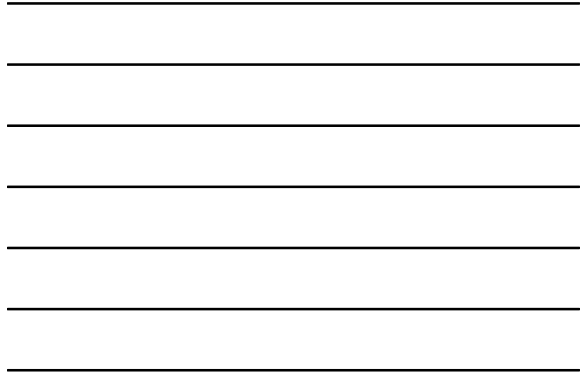
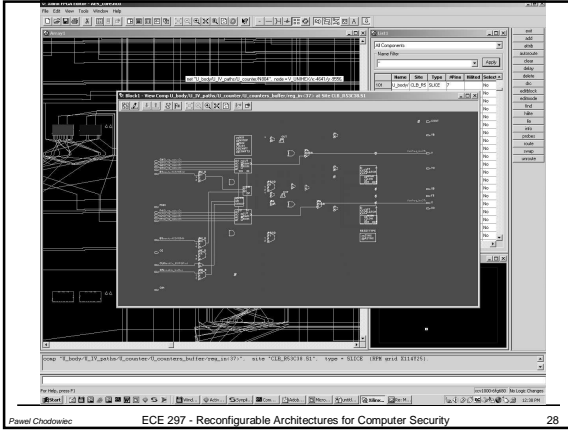




FPGA Editor

- Very powerful surgical tool
- Can change any configuration detail of FPGA
 - Placement of components
 - Configuration of CLB Slices
 - Routing of particular nets





Timing Analyzer

- Performs static analysis of the circuit performance
- Reports critical paths with all sources of delays
- Determines maximum clock frequency



The screenshot shows the Timing Analyzer report in Xilinx ISE. It includes a table of delays for various paths, such as 'Data Path' and 'Data Path - sensitive clock skew'. The report also includes a summary of the total delay and the maximum clock frequency.

Path	Delay (ns)	Source
Data Path	22.330ns	clock2_0FF0E0E0
Data Path - sensitive clock skew	14.17ns	clock2_0FF0E0E0

